REMARKS

The Office Action dated March 24, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 3-7 of the present application.

By this Amendment, the specification, the drawings, and claim 1 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-9 are pending in the present application and are respectfully submitted for consideration.

The drawings were objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because they include reference signs not mentioned in the description. Applicants respectfully present herewith replacement Figures 2, 3, 4, 6, 10 and 11 which include the desired changes, without markings, and which comply with §1.84(p)(5). The timing chart of Fig. 3 is parallel to the timing chart of Fig. 2. Since the timing chart of Fig. 3 is described in comparison with the timing chart of Fig. 2, it is submitted that a written description directed to Fig. 3 may be derived from the written description of Fig. 2.

In conjunction with the replacement Figures, the specification has also been amended to include written descriptions of the reference signs appearing in the drawings with the desired changes. Thus, Applicants respectfully request consideration of amended Figures 2, 3, 4, 6, 10 and 11.

Claim 1 was rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, claim 1 was rejected because Figure 1 allegedly fails to show the structural elements as recited in the claim.

Applicants respectfully traverse this rejection. As shown in Fig. 1, a dummy cell capacitor is electrically coupled to a bit line while a memory cell capacitor is electrically coupled to the other bit line. As such, the reading of data from a memory cell capacitor to a bit line is associated with the coupling of a dummy cell capacitor to the other bit line. In other words, the read operation of the present invention can be performed, for example, by the structural recitation of the memory cells coupled to the first bit line and a dummy cell coupled to the second bit line. Thus, Applicants submit that claim 1 recites subject matter that is fully described in the specification in such a way to enable one skilled in the art to which it pertains, to make and/or use the invention. Withdrawal of the rejection is respectfully requested.

Claims 1, 2, 8 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kitamoto et al. (U.S. Patent No. 5,889,718, hereinafter "Kitamoto"). Applicants respectfully submit that each of claims 1, 2, 8 and 9 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor memory device comprising a plurality of bit line pairs, each of which includes a first bit line and a second bit line, a plurality of memory cells which are coupled to said first bit line, and include capacitors that store electric charge, a dummy cell which is coupled to a second bit line, and includes a dummy

capacitor that is charged with a predetermined potential. The dummy capacitor is electrically connected to the second bit line during a period that overlaps a period during which one of the capacitors is electrically connected to the first bit line. In addition, the semiconductor memory device includes a sense amplifier, which amplifies a potential difference between the first bit line and the second bit line, and a control circuit which charges said dummy capacitor with the predetermined potential only for a fixed time period.

Accordingly, at least one of the essential features of the present invention is "a dummy cell which is coupled to a second bit line, and includes a dummy capacitor that is charged with a predetermined potential, said dummy capacitor being electrically connected to the second bit line during a period that overlaps a period during which one of the capacitors is electrically connected to the first bit line." As such, the present invention results in the advantage of having a semiconductor memory device operating based on the dummy-cell method in which a stable read operation is achieved regardless of access intervals.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 1, 2, 8 and 9, and therefore fails to provide the advantages that are provided by the present application.

Kitamoto discloses a dynamic type semiconductor memory device that includes a sense amplifier connected between complementary bit lines on which memory cells are connected, dummy cells each connected on at least one bit line and having a charge accumulation node or a node, at which charge is accumulated, to be linked to the bit line when selected, and a circuit for controlling the potential at a charge accumulation

node in a dummy cell during a precharge period during which the complementary bit lines are precharged, so that the potential at the bit line will be set to a given potential. The given potential of Kitamoto is set to a potential lower than an intermediate potential of the potential at a high-potential power supply and the potential at a low-potential power supply attained when a potential difference between the complementary bit lines is amplified by the sense amplifier.

Applicants respectfully submit that each and every element recited within claim 1 is neither disclosed nor suggested by Kitamoto. In particular, Applicants submit that the semiconductor memory device as recited in the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limitation of "a dummy cell which is coupled to a second bit line, and includes a dummy capacitor that is charged with a predetermined potential, said dummy capacitor being electrically connected to the second bit line during a period that overlaps a period during which one of the capacitors is electrically connected to the first bit line."

It is submitted that Kitamoto merely charges a charge-storage node of a dummy cell to a voltage V1 (ground voltage), and couples the dummy cell to a pair of bit lines coupled together after the bit lines are sensed to H and L, respectively, through data-read operation, thereby pre-charging the bit lines below the midpoint potential between H and L. Furthermore, Kitamoto provides that the charge-storage node of the dummy cell coupled to the bit lines is coupled to a voltage V2.

More importantly, Figure 3 of Kitamoto discloses that the dummy cell is coupled to the bit lines <u>when a word line is not activated</u>. (Emphasis added.) In contrast, the present invention provides that the dummy capacitor is electrically connected to the

second bit line during a period that overlaps a period during which one of the capacitors is electrically connected to the first bit line. In this manner, the function and operation of the dummy cell of the present invention is neither comparable nor analogous to that which is shown in Kitamoto. Accordingly, Kitamoto fails to disclose or suggest each and every element recited in claim 1 of the present application, and therefore is allowable.

Applicants further traverse the rejection of claims 8 and 9. As indicated in item no. 6 of the Office Action, claims 3-7 contains allowable subject matter. Each of claims 8 and 9 depends from allowable claim 7, and therefore incorporates all the allowable subject matter in claim 7. Therefore, claims 8 and 9 are allowable.

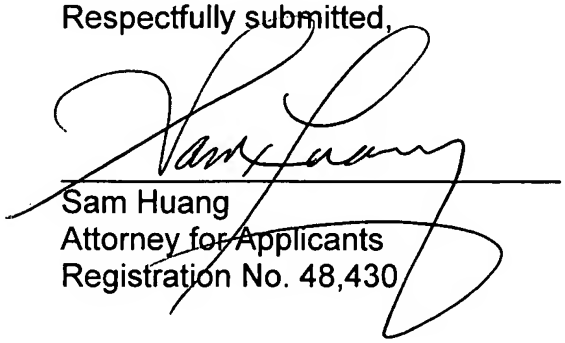
In addition, as claims 2, 8 and 9 depend from claim 1, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims.

In view of the above, Applicants respectfully submit that each of claims 1, 2, 8 and 9 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully request that claims 1, 2, 8 and 9 be found allowable along with allowable claims 3-7 and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 100353-00175.**

Respectfully submitted,



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Enclosures: Replacement Figures 2, 3, 4, 6, 10 and 11

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